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Implementation of Content Addressable Memory using MSML Architecture

Pravallika Gutta [1], Sreenivasulu Mamilla [2]

M. Tech Student, ECE, GVPCOE (A), Vishakapatnam, India[1]

Assistant Professor, ECE, GVPCOE (A), Vishakapatnam, India [2]

Abstract: Content Addressable Memory is a storage unit built on hardware. It is majorly used in internet routers to access fast look up tables. Available techniques to build CAM are power inefficient as CAM implements parallel comparison unit in its design. This project has implemented the content addressable memory using Master-Slave Match Line architecture. In the Master –Slave configuration, the CAM word is divided into number of segments. Each segment is provided with an additional slave match lines along with one Master Match Line. This configuration reduces the voltage swing across the Match Line (ML). By reducing the voltage swing, the power consumption across the Match Line is reduced. Finally, 128x8 CAM memory is implemented. The CAM array is tested for different possible cases. When the data is given to the CAM array, it is searched simultaneously in the entire memory. The 128X8 CAM array is tested at both lower frequencies and higher frequencies**.**

Keywords: CAM; MSML design; 4T CAM; Match Delay; HSPICE.

I. INTRODUCTION

Content Addressable memory is one of the hardware storage unit which can be accessed faster than conventional memory unit. It is an outgrowth of Random Access Memory. CAM supports both read and writes operations just like RAM. Along with these it can also support search operation. During this search operation, CAM compares the given data with the data stored in the memory. When a match is found, then it will accesses the corresponding location and retrieves the data from that location. If multiple matches occur in single search operation, a priority encoder circuit is used to select highest priority data. CAM based lookup tables are very fast when compared to the available lookup techniques because of its parallel nature of search operation. In CAM memory Match Lines and Search Lines account for major power consumption. As per [2] and [3] they account for nearly 66%-85% of total power consumption and this paper main aim is to reduce it. Other techniques such as Segmented ML Architecture, Shadow ML design etc.

Were proposed to reduce the dynamic power consumption in the CAM. But all these schemes suffer from various disadvantages. These techniques use NOR type CAM architecture. We need another scheme which is both power efficient and high speed. Hybrid type CAM [4] is another technique which is used to reduce the power consumption. In this design, the NOR type CAM is combined with the NAND type CAM. The NAND type design will reduce the power consumption. Hence, total power consumption of the circuit is reduced. A selective precharge [5] technique has been developed to reduce the power consumption. In this method, the entire CAM word is divided into segments. A set CAM cells are used to determine whether ML should be precharged or not.

Another scheme called pipelined search scheme was developed in which each segment was evaluated sequentially. This selective precharge techniques were used in [6]-[10] but with little improvement. A pipelined scheme was proposed which will improve the search performance; it will give best performance in best case, which is when the first segment can prevent further comparison in next circuits. All the techniques described above use NOR-type ML architecture. In contrast, the PF-CDPD AND-type ML scheme [11] is a NAND-type ML design with low-power feature. Based on the PF-CDPD [11], various arrangements of ML segmentation, including the tree-style [12] and butterfly-style [13] could not improve the performance. In particular, Huang et al.[14] combined the butterfly ML with the multimode data-retention power gating, super cut-off power gating , and the hierarchy search-line scheme not only improve the performance, but also reduce the power consumption.

Conventionally, there are two types of architectures to connect ML to the circuit. They are NAND type and NOR type. The NOR type ML gives the better performance among two, but it gives very high power consumption.
But NAND type ML has low power consumption at the cost of low search performance. The ML power consumption can be reduced by reducing the voltage swing across the ML. There are different techniques for reducing the power consumption across Match line. Master – Slave ML (MSML) architecture is one technique which is used in this paper. This structure uses the charge refill minimization technique to reduce the voltage swing across the Match Line during switching. The circuit diagrams for conventional CAM cell is shown below.

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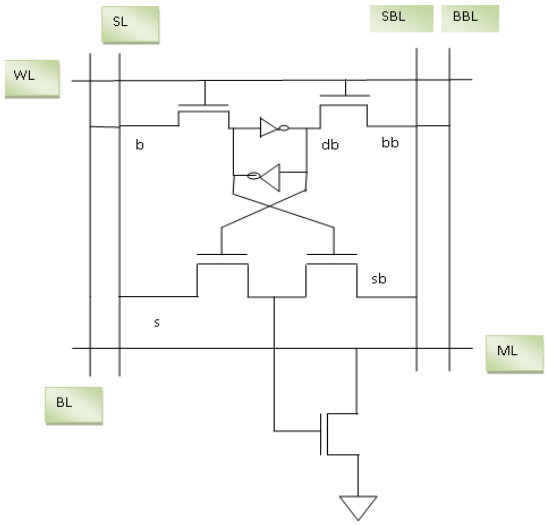

Fig.1. Conventional CAM Cell

Above circuit can store single bit. When word line is activated, data is written into the storage unit which comprises two inverters connected back to back. Data is loaded onto bit drivers and it is stored at the nodes d and db. When the data is to be searched it is loaded onto search lines. Here XOR logic is used in the comparison unit. Stored data is compared with the loaded data and the output of the comparison unit is given to the pull down transistor. Drain of the pull down transistor is connected to the Match line. Match line is initially precharged to $V_{DD.}$ If any mismatch occurs, then it output of XOR unit is high and it will turn on the pull down transistor. Then Match line is discharged to ground. If it is a match then Match line will retain its original value $V_{DD.}$

II. MASTER-SLAVE MATCH LINE DESIGN

The basic idea behind this design is charge refill minimization technique. This will reduce the Match Line power consumption. In this design entire CAM word is divided into number of segments. Each segment is provided with a Slave Match Line. Here the power consumption across Match Line is reduced by reducing the voltage swing on Match Line during charging and discharging of Match Line. When any miss match occurs in any one of the CAM cell, then the charge across the Match Line is distributed to the Slave Match Line to which the miss match CAM cell belongs. Then, during the next precharge cycle, the Match Line is charged to the V_{DD}, but the voltage swing reduces as the Match Line holds intermediate voltage value depending on the number of mismatched segments. By charge sharing, the Slave Match Lines will be charged to certain voltage value. This will turn on the pull down transistor to which the Final Match Line is connected. Then the Final Match Line will be discharged to ground when a mismatch occurs. The circuit for the MSML design is given in the figure 2.

WORKING OPERATION: For the analysis purpose the CAM word has been divided into two segments. A Slave Match Line is assigned to each segment. So, SML1 and SML2 correspond to segment 1 and segment 2 of the CAM word.

It operates in two phases

a) Precharge Phase
b) Evaluation Phase

PRECHARGE PHASE: During this phase the precharge signal PRE=1, so the Match Line is charged to V_{DD}. The Slave Match Lines SML1 and SML2 are discharged to ground through pull down transistors. Similarly the Final Match Line (FML) is also charged to V_{DD}. All the bit lines, search lines and word lines are reset to zero. Hence the share transistors will be turned off as the XOR output is zero.

EVALUATION PHASE: In this phase, the precharge signal is low i.e. PRE=0. The data to be written is loaded onto bit lines. The word line is high in this phase. So the data that appears on bit line is stored in the storage unit which is a SRAM. And then the data is compared with the stored data .As the CAM word is divided into two segments, it has two slave match lines, SML1 and SML2. There are four possible combinations depending on the match case. When both the SML's are a match then only we have a match case. All the four cases are discussed below.

CASE1 (Both SML's are match):
In this case both the segments are a perfect match. So none of comparison circuit will give logic one. Hence no charge sharing path is available for the match line. Thus the match line will retain its supply voltage $V_{DD.}$ Hence no discharging path will be available for final match line. So the final match line will show logic '1'.

CASE2 (One of SML's is a Mismatch):
In this case only one segment is a match. Suppose we assume that SML1 is a match and SML2 is mismatch. Then, in segment 2 there is at least one mismatch CAM cell. Hence there is at least one charge sharing path between Match Line and Slave Match Line. So there is an increase in the Slave Match Line voltage. When this voltage increases above the threshold voltage of the transistor then the pull down transistor is turned on. So the Final Match Line will be discharged to ground. The final balance voltage across the Match Line and Slave Match Line depends on the charge sharing equations given below.

$$V_B = \frac{C_{MML}}{C_{MML} + C_{SML\,1}} V_{MML} \approx \frac{2}{3} V_{MML}$$

Where C_{MML} is the capacitance of Master Match Line and C_{SML1} is the capacitance of Slave Match Line, V_B is the final balance voltage across Master Match Line and Slave Match Line, and V_{MML} is the initial voltage across Master Match Line. By roughly estimating the values of C_{SML1} and C_{MML}, we can get the final balance voltage as (2/3) $V_{MML.}$

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CASE3 (Both Segments are Mismatch):
Here both the segments are mismatch. This means there is at least one CAM cell in each segment which is a mismatch. Hence there is a charge sharing path between both Slave Match Lines and Master Match Line. So the charge across the Master Match Line is shared with Slave Match Line. Then the voltage across the Slave Match Line rises to the final balance voltage. This final balance voltage is determined by the charge sharing equation given below.

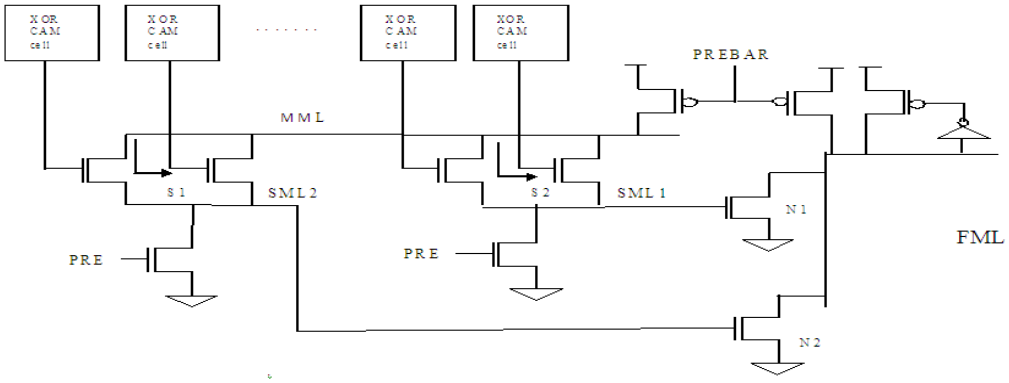

Fig.2. CAM using MSML Architecture

$$V_B = \frac{C_{MML}}{C_{MML} + C_{SML1} + C_{SML2}} V_{MML} \approx \frac{1}{2} V_{MML}$$

Here, C_{MML} is the capacitance of Master Match Line and C_{SML1}, C_{SML2} is the capacitances of Slave Match Line 1 and Slave Match Line 2. Here the final balance voltage is (1/2) V_{MML}. Among all the cases, the maximum power is consumed when both the segments are mismatch. This is because the final balance voltage is very low when compared with the first case. Hence the voltage swing is more, and so is the power. In all the previous techniques the power is reduced only in the best case. But when we consider the worst case performance, they consume enormous amounts of power. But this Master-Slave Design will reduce the power in all the cases. In the worst case, theoretically it reduces the power by nearly 50%. We have used HSPICE simulator to simulate the circuit and CADENCE tool to draw the layouts for the circuits.

III. SIMULATION RESULTS

HSPICE simulation tool is used to simulate the circuit. PTM 90nm technology is used for designing the circuit. It has been observed that the proposed technique has reduced the power consumption of the circuit. Layout for single CAM cell is drawn using CADENCE tool. Match delay is the performance metric used to determine the performance of the circuit.

It is defined as the time taken by the FML to discharge to zero in case of mismatch. Match delay for different configurations of Master –Slave design are shown below. All the results are simulated for 128 bit size word. It is observed that Match Delay for MS2 configuration is more when compared to other configurations. But the power consumption value for MS8 configuration is more when compared to other configurations. CAM array consisting 8 CAM words is implemented. Each word is used to store a single 128 bit word.

	MS2		MS4		MS8	
	1 miss	All miss	1 miss	All miss	1 miss	All miss
Match Delay(ns)	2.45	1.2	1.93	1.1	2.4	1
Power consumption in mw	2.8	2.87	3.03	2.82	3.04	2.8

Table.1. Average power consumption and Match Delay

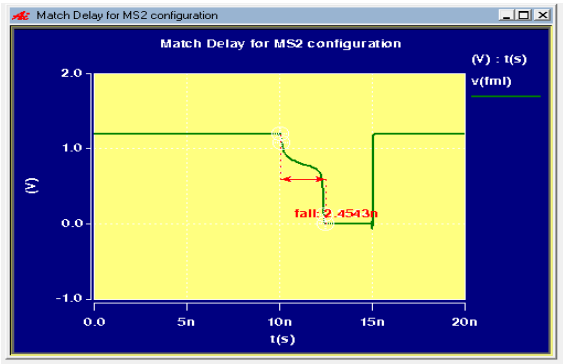

Fig.3. Match Delay for MS2 configuration

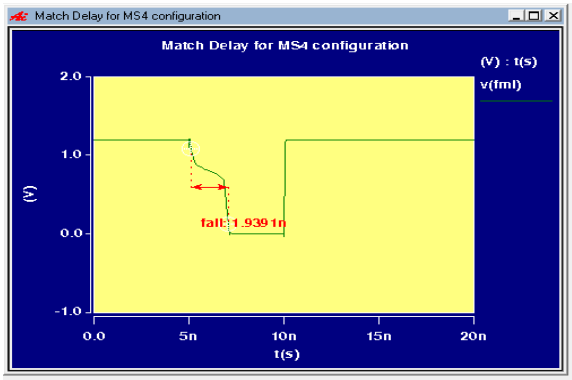

Fig.4. Match Delay for MS4 configuration

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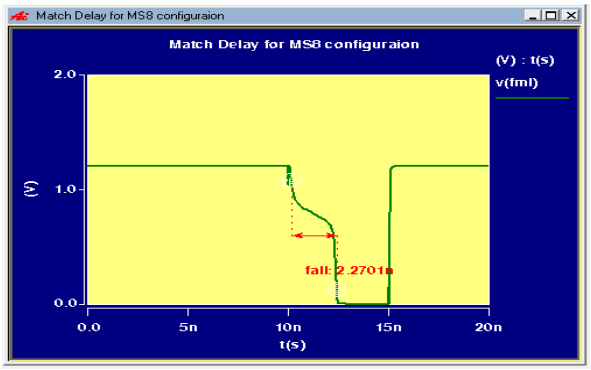

Fig.5. Match Delay for MS8 configuration

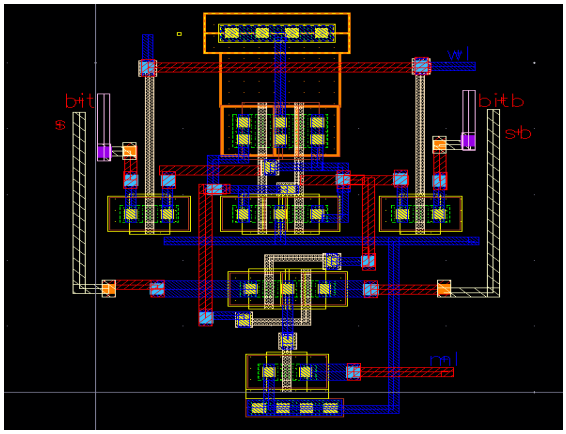

Fig.6. Layout for single CAM cell

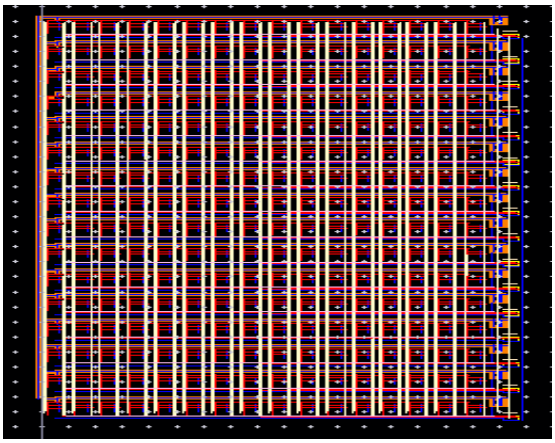

Fig.7. Layout for 16x16 CAM array

IV. CONCLUSION

This thesis uses the Master-Slave Match line architecture to design low power content addressable memory. CAM is a power hungry circuit. Major amount of power consumption is contributed by the Match Line. This architecture reduces the power consumption very effectively when compared to other available techniques. Simulation results obtained indicate that the power is reduced by nearly 50% in the worst case scenario. This thesis also implemented 128X8 CAM structure. Different test inputs were given to test the circuit under different circumstances. It was observed that all the words were searched simultaneously and no delay was reported in observing the final output. The circuit was also simulated at lower frequencies and higher frequencies. No changes in the performance were observed. The HSPICE simulation results show that this architecture works best for large size memory.

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